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H-706-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No. : 09/864,338 Confirmation No. 3538

Applicant : J. ETOH et al.

Filed : May 25, 2001

Title : LARGE SCALE INTEGRATED CIRCUIT WITH SENSE
AMPLIFIER CIRCUITS FOR LOW VOLTAGE OPERATION

TC/AU : 2827

Examiner : S. L. Mai

Customer No. : 24956

**SUPPLEMENTAL DECLARATION
FOR REISSUE PATENT APPLICATION**

MAIL STOP: Reissue
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

Sir:

As a below named inventor, I hereby declare that:

My citizenship, residence and post office address are as stated next to my name.

Kiyoo Itoh

Citizenship: Japan

Residence: Higashikurume, Japan

Post Office Address:

c/o Hitachi, Ltd. of Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, JAPAN,

In re Reissue Application of
K. Itoh et al
Serial No. 09/864,338
Supplemental Declaration

H-706-02

Yoshinobu Nakagome

Citizenship: Japan

Residence: Hachioji, Japan

Post Office Address:

c/o Hitachi, Ltd. of Kanda Surugadai 4-chome, Chiyoda-ku, Tokyo, JAPAN,

I believe I am the original, first and joint inventor of the invention described and claimed in U.S. Letters Patent No. 5,526,313 and in the specification of the foregoing reissue application and for which improvement is solicited a reissue patent.

IDENTIFICATION OF ERROR

The patentees had a right to claim all aspects of the invention. There is an error in that the patentees claimed less than they had a right to claim in the patent. Specifically, the patentees had a right to claim the embodiments of the invention shown in Figs. 12A-15C.

To correct the error through the present reissue application, applicants have submitted new claims 53-63, 65 and 70-74, which are supported by the original disclosure and drawings of the patent. With respect to the new claims, claims 53 and 70 are the independent claims.

Claims 53-63, 65 and 70-74 are supported by Figs. 12A-15C, which are discussed on pages 9-11 of the specification.

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With respect to claim 53, Fig. 15A shows complementary MISFETs including P-channel and N-channel MISFETs T_{33} , T_{32} and a circuit block 61 that also includes an operating voltage V_{CL2} . In a first operation mode, V_{P1} is at 0 volts. In the second operation mode, V_{BP1} is at -1 volts, as shown in Fig. 15C. Claim 70 is also supported by Fig. 15A and includes first and second circuit blocks 60, 61. Support for the remainder of the claims is provided by Figs. 12A-15C.

The error in claims 1 – 12 that is corrected by the present Reissue application is pointed out as follows. Claims 1 – 12 are directed to a sense amplifier driving circuit supported by Figures 73A – 78C of the Reissue application. Each of the independent claims 1, 5, 6, 8 and 9 includes a sense amplifier and common driving lines or a common driving line pair for driving the sense amplifiers. The limitations identified in each of independent claims 1, 5, 6, 8 and 9 of the original patent are not in pending claims 53 – 63, 65 and 70 – 74. The reason is that claims 53 – 63, 65 and 70 – 74 are directed to a different embodiment of the invention.

ERROR STATEMENT

Every error in the patent which was corrected in the present reissue application, and which is not covered by any prior declaration submitted in this reissue application, arose without any deceptive intention on the part of the Applicants.

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We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

9/18/2007
Date

Kiyoo Itoh
Kiyoo Itoh

Date

Yoshinobu Nakagome

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Date
9/19/2007
Date

Kiyoo Itoh
Yoshinobu Nakagome
Yoshinobu Nakagome